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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/997,019
Filing Date: November 28, 2001
Appellant(s): WHITMAN ET AL.

Brick G. Power
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on October 3, 2005 appealing from the Office action mailed May 12, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

U.S. Application No. 09/542,78.

U.S. Application No. 09/944,230.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The Appellants' statement of the status of amendments after final rejection contained in the brief is incorrect.

The after final amendment that was filed on July 14, 2005 under 37 CFR 1.116 has been considered but was not entered because the amendment did not either place the application in condition for allowance or place the application in better form for appeal by materially reducing or simplifying the issue for appeal as indicated in the advisory action mailed on July 26, 2005. In addition, the after final Office action and the advisory action addressed all the rejected claims, i.e., claims 1-22 not claims 1-17 as appellants indicated in page 5 line 2 of the brief.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The Appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon the rejection of claims under appeal.

6,461,932	**Wang**	**10-2002**
6,228,711	**Hsieh**	**5-2001**
6,117,486	**Yoshihara**	**9-2000**

(9) Grounds of Rejection

The following ground(s) of rejection are applicable the appealed claims:

a. Claims 1, 2, 6, 7, and 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (US/6,461,932).

Re claim 1, Wang discloses a method for preparing a surface of a semiconductor device structure for planarization, comprising: providing a semiconductor device structure (see Fig. 4d) including at least one recess (54) (i.e., trench in the silicon substrate (40)) formed in a surface thereof and a first material layer (56) substantially filling the at least one recess (54) and covering the surface (not labeled), the first material layer (56) having a non-planar surface (see Fig. 4d); applying a second material (60) to the first material layer (56); and spreading the

second material (60) over the first material layer (56) so as to forming a second material layer (60) having a substantially planar surface (see Col. 6, lines 29-37) without requiring subsequent planarization of the second material (see Fig. 4d).

Re claim 2, as applied to claim 1 above, Wang discloses all the claimed limitations including the limitation wherein the applying said second material comprises applying a stress buffer material to the first material layer (see Fig. 4d).

Re claim 6, as applied to claim 1 above, Wang discloses all the claimed limitations including the limitation wherein said providing comprises providing a shallow trench isolation structure with the at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure (see Fig. 4d).

Re claim 7, as applied to claim 6 above, Wang discloses all the claimed limitations including the limitation providing the shallow trench isolation structure with the first material layer comprising an electrical insulator material (see Figs. 4d-4g).

Re claim 10, as applied to claim 2 above, Wang discloses all the claimed limitations including the limitation wherein the spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of said first material layer substantially uncovered by the stress buffer material (see Figs. 4d and 4e).

Re claim 11, as applied to claim 10 above, Wang discloses all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 4d and 4e).

Re claim 12, as applied to claim 11 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises etching at least one region of the first

material layer exposed through the stress buffer material with selectivity over the stress buffer material (see Figs. 4d and 4e).

Re claim 13, as applied to claim 12 above, Wang discloses all the claimed limitations including the limitation wherein said etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material (see Figs. 4d and 4e).

Re claim 14, as applied to claim 13 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing further comprises abrasively planarizing the stress buffer material and the at least one region to expose the surface of said semiconductor device structure adjacent the at least one recess, said surface of the semiconductor device structure and a surface of thefirst material layer in the at least one recess being located in substantially the same plane following said planarizing (see Figs. 4d and 4e).

Re claim 15, as applied to claim 13 above, Wang discloses all the claimed limitations including the limitation wherein said plananizing further comprises concurrently etching said first material layer and the stress buffer material at substantially the same rate so as to expose said surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of said first material layer in the at least one recess being located in substantially the same plane following said plananizing (see Figs. 4d-4f).

Re claim 16, as applied to claim 11 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing is effected until said surface of said semiconductor device structure is exposed through the first material layer (see Figs. 4d-4e).

Re claim 17, as applied to claim 16 above, Wang discloses all the claimed limitations including the limitation wherein the etching is effected until a surface of the first material layer in the at least one recess is in substantially the same plane as the surface of said semiconductor device structure (see Figs. 4d-4f).

Re claim 18, as applied to claim 16 above, Wang discloses all the claimed limitations including the limitation removing the stress buffer material from the semiconductor device structure (see Figs. 4d-4f).

Re claim 19, as applied to claim 2 above, Wang discloses all the claimed limitations including the limitation wherein the spreading comprises forming a substantially planar surface over the semiconductor device structure (see Figs. 4d-4f).

Re claim 20, as applied to claim 19 above, Wang discloses all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 4d-4f).

Re claim 21, as applied to claim 20 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises substantially concurrently abrasively planarizing the stress buffer material and the first material layer to surface of said semiconductor device expose the device structure adjacent the at last one recess, said surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following the planarizing (see Figs. 4d-4f).

Re claim 22, as applied to claim 20 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises substantially concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of said semiconductor device structure adjacent the at least one recess with said surface

of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following said planarizing.

b. **Claims 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Wang (US/6,461,932) in view of Yoshihara (US/6,117,486).**

Re claims 3-5, as applied to claim 1 above, Wang discloses all the claimed limitations. Although is a well-known process, Wang does not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Wang reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

c. **Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Wang (US/6,461,932) in view of Hsich (US/6,228,711).**

Re claims 8 and 9, as applied to claim 1 above, Wang discloses all the claimed limitations. Although it is well-known in the art, Wang does not specifically disclose providing dual-damascene structure.

Hsich discloses forming of dual-damascene structure and forming a conductive layer over the dual-damascene structure (see Fig. 3H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Wang reference with dual-damascene structure as taught by Hsich. because, as well-known in the art, the structure would have increased the device density.

(10) Response to Argument

Appellants' arguments in the brief that was filed on October 3, 2005 have been fully considered but they are not persuasive.

I.

A.

Appellants argue that, in Pages 9-10, with respect to claims 1, 6, 7, and 10-22,"Wang lacks any express or inherent description of spreading a second material layer over a first material layer so as to form a second material layer having a planar surface, as recited in independent claim 1. Contrary to the assertion that has been made at page 11 of the Final Office

Action, a *largely planar* surface 62 that may include *slight depressions* is not planar...Wang does not anticipate *spreading* [a] second material over [a] first material layer having a planar surface...,"

In response to Appellants' argument, it is respectfully submitted that the argument is not commensurate with the scope of the rejected claims. As set forth in Paragraph 9(a) above, Wang '932 teaches all the claimed limitation including the limitation *spreading a second material layer over a first material layer so as to form a second material layer having a planar surface,* as recited in claim 1. In addition, the claimed invention is not distinguishable from Wang '932 disclosure, and appellants do not specify in the claims the type of material that is deposited to form the first material and second material layers.

In order to fully respond to Appellants' description of Wang '932 expression "largely planar", the instant application claimed invention, particularly to the meaning of "planar," should be considered in light of Appellants' disclosure. Since it is relevant to the instant application, also as pointed out by the Appellants in the summary of invention in page 5 of the brief, Fig. 7 of the instant application is reproduced below for demonstrative purpose.

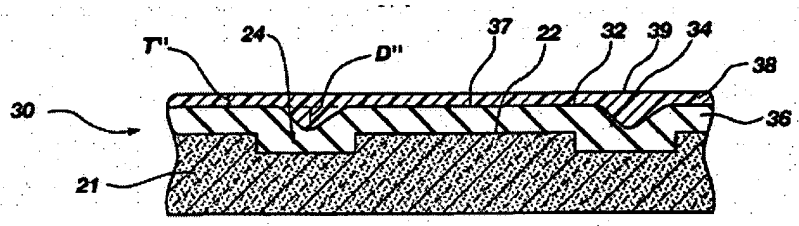


Fig. 7

As shown above, Applicants' own drawing that the basis of support for the claimed invention of the instant application, Fig 7 is neither in scale nor 100 % "planar" in every where

in the surface of the layer 36. There is no support can be found in the Applicants' own disclosure that describe degree of planarization.

In determining the scope of the claims, the claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Also see *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). Also See *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

As depicted above, the first material **36** fills the trenches **24**, and the first material **36** has non-planar surface upper surface **37** which includes valleys **34** (see Paragraph 0045 of the instant application). The second material **38** is deposited to fill cover the first layer **36**. In addition, the second material **38** is formed by a spin-coating process (see Paragraph 0046 and Paragraphs 0039-0041) to form a planar second material **38** layer as depicted in Fig. 7.

In this regard, the Examiner respectfully would like to point out Applicants' specification in Page 15, paragraphs [0045] through [0046], as shown below, the stress buffer layer 38 is "substantially planar." The only interpretation can be given to the meaning of "planar," as clamed in claim 1, is "substantially planar," as described in the Appellants' own specification.

[0045] Referring now to FIGs. 7-11, a second shallow trench isolation structure 30 embodiment of a semiconductor device structure according to the present invention is illustrated. With reference to FIGs. 7 and 8, shallow trench isolation structure 30 includes a semiconductor substrate 21 with a surface 22 and trenches 24 recessed, or formed in, surface 22. A layer of electrically nonconductive material, or insulator layer 36, substantially fills trenches 24 and covers surface 22. Insulator layer 36 has a nonplanar upper surface 37 and includes valleys 34 located substantially above trenches 24 and peaks 32 located substantially above surface 22.

[0046] Shallow trench isolation structure 30 may also have a layer 38, 38' of stress buffer material, which is also referred to herein as a stress buffer layer, having a substantially planar surface 39, 39' disposed at least partially over insulator layer 36. FIG. 7 illustrates stress buffer layer 38, which substantially fills valleys 34 recessed in insulator layer 36 and substantially completely covers peaks 32. The thickness T" of regions of stress buffer layer 38 located above peaks 32 is less than the depths D" of valleys 34. Thickness T" is preferably less than about half of depth D". FIG. 8 depicts stress buffer layer 38', which does not extend over peaks 32 and which may only partially fill valleys 34. Stress buffer layers 38, 38' are preferably formed from a photoresist or other polymer by processes the same as or similar to those disclosed previously herein with reference to the fabrication of mask layer 18 illustrated in FIG. 2.

Similarly, Wang '932 discloses a process substantially as claimed, as depicted Fig. 4d below.

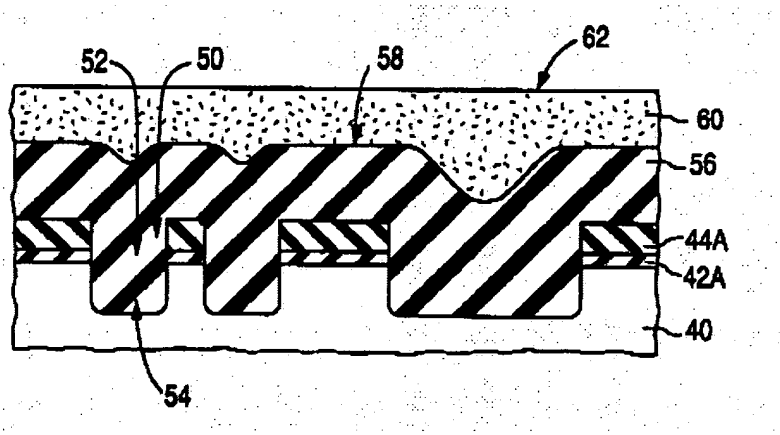


Fig. 4d

As shown in Fig. 4d above, Wang '932 discloses providing a semiconductor device structure including at least one recess **54** (i.e., trench in the silicon substrate **40**) formed in a surface thereof and a first material layer **56** (i.e., an insulation layer) substantially filling the at least one recess **54** and covering the surface (not labeled), the first material layer **56** having a

non-planar surface; applying a second material **60** to the first material layer **56**; and spreading the second material **60** (i.e., spin coating process, see Col. 6) over the first material layer **56** so as to form a second material layer (60) having **a planar surface** (see Col. 6, lines 29-37) **without requiring subsequent planarization** of the second material (i.e., no polishing process conducted to planarize second material layer **60**). In particular, Wang '932 also disclose that the second material layer **60** can be created by a "deposition/spinning" procedure (i.e., spin-coating process) (see Col. 6, lines 52-64). In addition, as shown above, second material layer **60** has planar surface **62** and which is similar to that of the instant application claims.

Wang '932 also disclose the possibility of "slight depression" in the second material layer **60** in the region of the deepest part of the depressed portion upper surface **58** of the first layer **56**. (See Wang '932 Col. 6, lines 29-36). In this regard, Appellants' own disclosure does not eliminate that the possibility of the existence of "slight depression" that is resulted form the valleys. If there such evidence existed, it would have been apparent form Appellants' own disclosure. Therefore, there is no intrinsic or extrinsic evidence is presented by Appellants' such that theirs invention avoids "slight depression" that what is noted by Wang '932.

> Importantly, smoothening layer **60** has an upper surface **62** which is considerably smoother than upper dielectric surface **58**. Ideally, upper smoothening surface **62** is largely planar. In actuality, there may be slight depressions in upper smoothening surface **62** at the locations of the deepest parts of the depressed portion of upper dielectric surface **58**. Compared to upper dielectric surface **58**, upper smoothening surface **62** is largely planar.

In addition, Wang '932 disclosure indicates that "largely planar" means planar. Alternatively, because the instant application does not specifically claim that the second material layer **38** is uniformly planar on the entire surface of the first material layer **36**, the claim reasonably reads on Wang's '932 description that "largely planar" is "planar" surface. In

addition, Appellants' specification discloses that the second material layer **38** (i.e., stress buffer layer **38**) is "**substantially planar**" (see the instant application specification Page 15, Paragraph 0047). The term "**substantially planar**" is analogous to "**largely planar**" as disclosed by Wang '932.

Furthermore, the term "spreading" does not have any special meaning. Therefore, the term "spreading" is interpreted according to Merriam-Webster online dictionary as set forth herein below.

Merriam-Webster Online Dictionary

Thesaurus

4 entries found for spread.
To select an entry, click on it.

spread[1,verb]
spreading factor
wide-spreading
seafloor spreading
Go

Main Entry: [1]**spread**
Pronunciation: 'spred
Function: *verb*
Inflected Form(s): **spread; spread·ing**
Etymology: Middle English *spreden,* from Old English *-spr[AE]dan;* akin to Old High German *spreiten* to spread
transitive senses
1 a : to open or expand over a larger area <*spread* out the map> **b** : to stretch out : EXTEND <*spread* its wings for flight>
2 a : to distribute over an area <*spread* fertilizer> **b** : to distribute over a period or among a group <*spread* the work over a few weeks> **c** : to apply on a surface <*spread* butter on bread> **d (1)** : to cover or overlay something with <*spread* the cloth on the table> **(2)** *archaic* : to cover completely **e (1)** : to prepare or furnish for dining : SET <*spread* the table> **(2)** : SERVE <*spread* the afternoon tea>

As depicted in Fig. 4d above, and described the spin-coating process above the Wang '932 discloses forming second material **60** to the first material layer **56**; and spreading the second material **60** (i.e., spin coating process, see Col. 6,) over the first material layer **56** so as to form a second material layer (60) having **a planar surface or substantially planar surface** (see Col. 6, lines 29-37).

In addition, in this case, "stress buffer layer" is the material used to reduce damage, i.e., to reduce dishing effect, on the first material layer during chemical-mechanical polishing (CMP) process of the first layer in order to form planar shallow trench isolation (see Wang '932 Col. 3, line 1 through Col. 4, line 17). The instant application claimed invention apparently avoids damage to the insulator layer **36** by providing the stress buffer layer **38** (see the instant application Page 16, Paragraph 0047) during the polishing process. The second material layer **60** (smoothing layer) disclosed by Wang '932, as depicted in Fig. 4d above, is also a stress buffer layer because Wang '932 also avoid damage to the insulating layer during formation of the planar (flat) STI (shallow trench isolation) by CMP process, i.e., the art recognized problem of "dishing." (See Wang '932 Col. 7, line 15 - Col. 8, line 56).

Further, with respect to Appellants' argument "Vand Zandt" reference in Page 10, it is respectfully submitted that reference has no relevancy for the issue in hand whether or not the instant application claimed invention is novel or non-obvious in view of the outstanding rejection as set forth in Paragraph 9 above. Therefore, with regard to "Vand Zandt" reference, Appellants' argument is moot.

Pertaining to claims 2, 6, 7 and 10-22, Appellants further argue that the claims allowable, among other reasons, because being depending the allowable claim, claim 1 (see the brief in Page 10 of last paragraph). In response Appellants' argument, it is respectfully submitted that claims 2, 6, 7 and 10-22 are not allowable because the base claim, i.e., claim 1, is not allowable. In addition, as set forth in Paragraph 9(a) above, all the claimed limitations of claims 2, 6, 7 and 10-22 are anticipated by Wang '932.

With respect to claim 10, Appellants argue that "Wang does not expressly or inherently describe the claimed subject matter recited in claim 10, i.e., wherein spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of said first material layer substantially uncovered by the stress buffer material..."

According to Appellants' own specification, the second material layer (i.e., the stress buffer layer) **38** is deposited on the surface of the first material layer (i.e., insulating layer) **36** by spin-coating process (see the instant application specification Page 8, Paragraph 0018 through Page 9, Paragraph 0022). In order to deposit a material on a surface by the spin-coating process, the material is deposited on the central potion of the surface while the surface is rotated. During the spinning operation, the material spreads out over the surface from the center to the periphery of the wafer and this is governed by Newton's first law of motion (i.e., circular motion). Therefore, initially some of the surface does not receive the coating material, but eventually all the surface is uniformly coated as a result of the spinning operation. This process also is within the scope of Wang '932 disclosure as depicted in Fig. 4d above.

In this regard, appellants' own disclosure does not provide any process that is distinguishable form that of Wang's '932 teachings.

As depicted in Figs. 8 and 9, the instant application shows that the exposed portion of the surface **37** of the first material layer **36** is formed by removing the second material layer **38** after the spin-coating process of Fig. 7. This is also within the scope of Wang '932 disclosure as depicted on Fig. 4e.

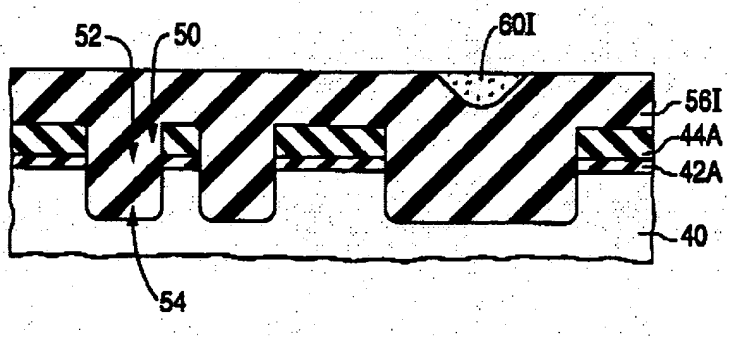
Pertaining claim 13, Appellants argue that "Wang includes no express or inherent description that the dielectric layer 56 may be etched with selectivity over the smoothening layer 60 thereof until a surface of at least one region of the dielectric layer 56 is in substantially the same plane as a surface of the smoothening layer 60..."

In response to Appellants' contention, it is respectfully submitted that appellants' characterization of Wang '932 teaching is not convincing for the flowing:

Claim 13, which depends from claim 12, recites the limitation "wherein the planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material; wherein said etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material."

As shown above, there is no particular type of etching process claimed in the rejected claim. The CMP process disclosed by Wang '932 etches some region of the first material layer **56** with selectively over the second material (stress buffer material) **60** until some of the region of the first material **56** becomes planar with the stress buffer material as clearly depicted on Fig. 4e below.

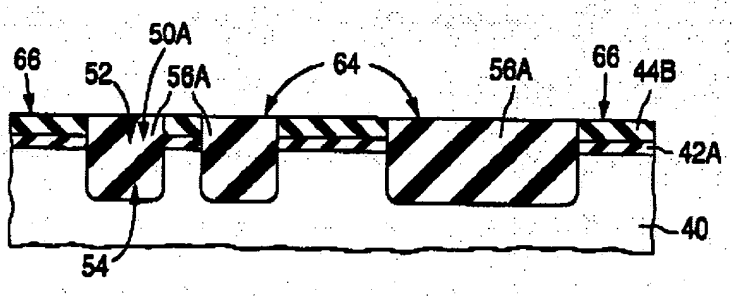
Fig. 4e



With respect to claim 15, Appellants argue that "Wang includes no express or inherent description that the dielectric layer 56 and the smoothening layer 60 may be etched at substantially the same rate so as to expose a surface of the mask layer 44 adjacent a surface of a portion of the dielectric layer 56 in at least one recess, with the surfaces of the mask layer 44 and the dielectric layer 56 being located in substantially the same plane following such planarization ..."

In response to Appellants' argument, it is respectfully submitted that, as explained above for claim 13, appellants do not specifically recited in the claim any particular type of etching process for removing both the first material layer **36** and the second material layer **38**. In addition, the CMP process of Wang '932, which utilizes chemical and mechanical polishing, is an etching process. As depicted in Fig. 4f below, Wang '932 teaches concurrent etching the first material layer **56I** and the second material layer **60I** of Fig. 4e (see Fig. 4e in previous page) in order to achieve a planar isolation structure of Fig. 4f as depicted below.

Fig. 4f



Hence, Wang '932 discloses all the claimed limitations including the limitation wherein said plananizing further comprises concurrently etching said first material layer and the stress buffer material at substantially the same rate so as to expose said surface of the semiconductor

device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of said first material layer in the at least one recess being located in substantially the same plane following said plananizing. Therefore, appellants' contention that Wang '932 does not explicitly or inherently teach the claimed limitation of claim 15 is not persuasive.

As demonstrated above, Wang '932 teaches all the claimed limitations of claims 1, 2, 6, 7, and 10-22 and the rejection under 35 U.S.C. § 102 is deemed proper.

B.

Pertaining to Appellants' argument in Pages 14-15, with respect to claims 3-5, i.e., "the Office has not established a prima facie case of obviousness ..."

In response to appellants' argument, it is respectfully submitted that claims 3-5 are not allowable, as demonstrated above, because claim 1 is not allowable. Furthermore, the combination of Wang '932 and Yoshihara '486 would have suggested to one of ordinary skill in the art applying the material to the surface of the semiconductor device structure; spinning the semiconductor device structure; decreasing the rate of spinning, while allowing the material to cure gradually; and finally increasing the rate spinning; exposing the material to a soft balling temperature; spinning the wafer at a rate of 1000 and 100 rpm (see Yoshihara '486 Figs. 10 and Col. 13, lines 25-44).

Both Wang '932 and Yoshihara '486 teachings are directed to coating of material on a substrate for the purpose of fabricating semiconductor device. Therefore, the teachings of Wang '932 and Yoshihara '486 are analogous. It would have been within the scope of ordinary skill in

the art to combine the teachings of Wang '932 and Yoshihara '486 in order to modify spin the coating process of Wang '932 by adjusting the spinning rate (rpm) according to the teachings of Yoshihara '486 because one having ordinary skill in the art would have been motivated to look to analogous art teaching alternative spin coating process such as the teachings of Yoshihara '486. In addition, the rationale to combine the references can be found in Yoshihara '486 Col. 13, line 26 - Col. 14, line 67. The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. See *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

C.

Pertaining to appellants' argument in Page 15, with respect to claims 8 and 9, i.e., "claims 8 and 9 are allowable because claim 1 is allowable ...," it is respectfully submitted that claims 8 and 9 should fall with claim 1 for the reasons indicted in Paragraph 10(IA) above. It is respectfully submitted that the combination of Wang '932 and Hsieh '711 teach all the limitations of Claims 8 and 9 of the instant application as discussed in Paragraph 9(c) herein above.

Therefore, the *prima facie* case of obviousness burden has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Finally, it is respectfully submitted that the recent ruling of the Federal Circuit Court, in *Playtex Products Inc. v. Procter & Gamble* Co., 73 UPSPQ2D 2010, 2015 (CFC 2005), i.e., with respect to the meaning of "substantial" or "substantially planar" (i.e., as described in the Appellants' own specification to the scope and the meaning of "planar surface" as claimed in the claims), should be considered in determining of patentability of the instant application claimed invention.

Respectfully submitted,

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER

Appeal conference has been held on December 8, 2005. The Conferees listed herein below.

1. Drew A. Dunn, Chair Person and SPE Art Unit 2872
2. Matthew S. Smith, SPE Art Unit 2823 MS
4. Brook Kebede, Examiner Art Unit 2823 BK 12/10/05

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December 10, 2005